REMARKS

Responsive to the Office Action mailed on September 21, 2006 in the above-referenced application, Applicant respectfully requests amendment of the above-identified application in the manner identified above and that the patent be granted in view of the arguments presented. No new matter has been added by this amendment.

Present Status of Application

Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1 and 5-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prall et al (US 2004/0130934, hereinafter "Prall").

In this paper, claim 1 is amended to recite the step of forming bit line insulating layers simultaneously by thermal oxidation over each of the doped areas. Furthermore, "conformable oxide layer" is amended to "conformable layer" and "insulating layer" is amended to "conformable layer." Claims 1 and 2 are amended to recite "doped area" in place of "doping area" for proper antecedent basis. Claims 7-9 are amended to correspond with the amendment to claim 1. Claim 5 is canceled. Support for the amendments can be found, for example, in original claim 5, page 6, lines 6-13 of the specification, and Fig. 2e of the application. Thus, on entry of this amendment, claims 1-4 and 6-12 remain in the application.

Reconsideration of this application is respectfully requested in light of the amendments and the remarks contained below.

Information Disclosure Statement

As noted on page 2 of the IDS filed on May 9, 2006 and supported by the attached Return Receipt Postcard (Attachment A), the reference CN 1189919A was accompanied by the abstract of US 5,998,261, which is a corresponding English-language application to CN 1189919A. As noted in MPEP 609.04(a)III, an English-language equivalent application and/or

an English-language abstract of a reference may fulfill the requirement for a concise explanation.

Applicant is resubmitting the IDS filed on May 9, 2006 with the listing of US 5,315,142 to Avovic removed. Applicant respectfully requests that the Examiner indicate that she has considered the information disclosed the statement by returning a copy of the Form PTO-1449 submitted therewith with her initials or other appropriate mark beside each listed reference.

Rejections Under 35 U.S.C. 112

Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the Examiner indicates that "the insulating layer" lacks antecedent basis.

As noted above, claim 1 is amended to recite "conformable layer" in place of "insulating layer." Applicant submits that the rejections under 35 U.S.C. 112 are thereby overcome.

Rejections Under 35 U.S.C. 103(a)

Claims 1 and 5-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prall. To the extent that the grounds of the rejections may be applied to the claims now pending in this application, they are respectfully traversed.

Applicant first notes that while the rejections are over Prall (US 2004/0130934), the office action also refers to "Forbes" on pages 4-5. Applicant further notes that two references to "Forbes" have been cited by the Examiner in the prosecution of this application, namely US 2003/0235079 listed in the Notice of References Cited mailed on August 24, 2005 and US 6,853,587 listed in the Notice of References Cited mailed on March 27, 2006. Applicant respectfully requests that the Examiner specify which reference is being referred to in any future action.

None of the cited references teach or suggest a method for fabricating a multi-bit vertical memory cell including a step of simultaneously forming bit line insulating layers by thermal oxidation over each of the doped areas, as recited in claim 1.

MPEP 2142 reads in part:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

In connection with the third criteria, MPEP 2143.03 goes on the state:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Claim 1 recites a method for fabricating a multi-bit vertical memory cell comprising the steps of:

> ... forming doped areas, acting as bit lines, in the semiconductor substrate 1) near its surface and 2) the bottom of the trench; and
>
> forming bit line insulating layers simultaneously by thermal oxidation over each of the doped areas ....

Prall teaches a method of forming a memory cell. In the office action, the Examiner identifies doped regions 24 and 26 as the alleged "doped areas" of claim 1. With reference to Fig. 1 of Prall, doped regions 24 are presumably the alleged "doped areas" near the surface while doped regions 26 are the alleged "doped areas" at the bottom of the trench. The Examiner further identifies caps 28, thick oxide regions 32, and thin oxide 42 as the alleged "bit line insulating layers" of claim 1.

Prall discloses caps 28 are first formed by conventional patterning techniques over the alleged "doped areas" 24 (see FIG. 1 and paragraphs 0028-0029), and then oxide regions 32 and 42 are formed by oxidation on the sidewalls 36 and over the doped regions 26 (see FIG. 2 and paragraph 0030-0031, e.g., "at a later stage in processing").

Thus, in Prall's method, the alleged "bit line insulating layer" 28 is formed by convention silicon nitride and patterning techniques over the alleged "doped areas" 24 near the surface. To the contrary, claim 1 recites that the bit line insulating layers are formed by thermal oxidation.

Furthermore, in Prall, the alleged "bit line insulating layers" 32 and 42 are formed in subsequent steps by oxidation over the alleged "doped areas" 26 at the bottom of the trench. Thus, the alleged "bit line insulating layers" 28, 32, and 42 are formed in sequential steps by different methods over each of the alleged "doped areas" 24 near the surface and the alleged "doped areas" 26 at the bottom of the trench. To the contrary, claim 1 recites a step of forming bit line insulating layers simultaneously by thermal oxidation over each of the doped areas.

Applicant finally notes that "Forbes" (whether US 2003/0235079 or US 6,853,587) also fails to teach or suggest a step of simultaneously forming bit line insulating layers by thermal oxidation over each of the doped areas.

It is therefore Applicant's belief that even when taken in combination, the prior art references relied upon by the Examiner do not teach or suggest all the limitations of claim 1. For at least this reason, a *prima facie* case of obviousness cannot be established in connection with this claim. Furthermore, as it is Applicant's belief that a *prima facie* case of obviousness is not

established for claim 1, the Examiner's arguments in regard to the dependent claims are considered moot and are not addressed here. Allowance of claims 1-4 and 6-12 is respectfully requested.

Conclusion

The Applicant believes that the application is now in condition for allowance and respectfully requests so. The Commissioner is authorized to charge any additional fees that may be required or credit overpayment to Deposit Account No. **502447**. In particular, if this response is not timely filed, then the commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 C.F.R. § 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to Deposit Account No. **502447**.

Respectfully submitted,

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ATTACHMENT A

Attorney Docket No. **10113741** Date: **May 9, 2006**
First Named Inventor: **Ching-Nan HSIAO**
Application No. **10/775,307**
Title of Invention: **MULTI-BIT VERTICAL MEMORY CELL AND METHOD OF FABRIATING THE SAME**

The following papers were received in the USPTO:

[X] Information Disclosure Statement (2 pages)
[X] Form PTO-1449 (1 page)
[X] Copies of listed references (1)
[X] English language abstract(s) (1)
[X] Copy of foreign office action (1)

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